Remarks:

Reconsideration of the application is requested.

Claims 3-8 are now in the application. Claims 3 and 5 have been amended. No new matter is believed to have been added. Claims 7-8 are withdrawn from consideration.

In the fourth paragraph on page 2 of the Office action, claims 3-6 have been rejected as being obvious over Muraoka et al. (U.S. Pat. No. 5,324,966) (hereinafter, "Muraoka") in view of and Harada et al. (U.S. Pat. No. 6,278,140 B1) (hereinafter, "Harada") and Obinata (U.S. Pat. No.5,341,003) under 35 U.S.C. § 103.

The rejections have been noted and the claims have been amended in an effort to even more clearly define the invention of the instant application.

Claim 3 calls for, inter alia, a semiconductor component, comprising:

another of said four doped regions being a second base region having a conductivity type with an opposite sign with respect to said given conductivity type, said second base region

extending as far as said first main side, having a channel and having said gate electrode for controlling said channel;

a further buffer layer being doped to have said given conductivity type and being disposed between said first base region and said second base region, a doping of said further buffer layer having a magnitude causing the semiconductor component to block in a direction from said drain contact toward said source contact in an envisaged range of opposite applied electrical voltages.

Accordingly, the present invention is directed to an IGBT structure including successive regions having conductivities of alternating signs. The structure is dimensioned for punch-through and is provided with two buffer layers. As a result, the component can symmetrically block, and is suitable as a semiconductor switch.

Further, in the present invention, the second base region extends as far as the first main side. In addition, the second base region has a channel, and a gate electrode for controlling the channel. Accordingly, the gate electrode (and not the second base region) controls the channel.

The Examiner asserts that Muraoka describes a weakly doped *first base region having a conductivity type with an opposite*

sign with respect to a given conductivity type. However, claim 3 of the instant application teaches that *the first base region has the given conductivity type.*

Moreover, Muraoka has only one buffer layer 3. See Fig. 1, Muraoka. A standard MOS-structure (in the thyristor) is provided on the main base side. Accordingly, Applicant points out that the layer 6 (which the Examiner considers as the second buffer layer) does not correspond to the second (further) buffer layer of the invention for the following reasons:

(1) According to amended claim 3 of the instant application, the further buffer layer is doped to have the given conductivity type (i.e., the same conductivity type as the first base region). In contrast, in Muraoka, the first buffer layer is n^+ doped, and the further buffer layer 6 is p doped. In other words, each of the "buffer layers" is respectively doped with (doping atoms of) a different conductivity type.

(2) The p-type layer 6 of Muraoka (which is denoted as a gate or a base region) only serves as a current-conducting part (for charge-injection from the cathode region 9 into the channel region 12).

In contrast, the further buffer layer of the *present invention* blocks (in reverse direction), so that the semiconductor component (of the *present invention*) can block in both directions. Muraoka does not teach or suggest such a component.

In addition, neither Harada nor Obinata teach or suggest a further buffer layer for reverse-blocking (i.e., blocking in a direction from the drain contact towards the source contact in an envisioned range of opposite applied electrical voltages).

Therefore, Applicant submits that, even if all of the three references were combined, a skilled artisan could not arrive at such a further buffer layer (as taught by the *present invention*).

Furthermore, the Examiner states that (the dimensioning of the doping of the) further buffer layer should be distinguished from the prior art in terms of structure (rather than function).

However, Applicant believes that (using the features of claim 3--with regard to the functions of the buffer layers) a skilled artisan will not have any problem in arriving at the correct doping dimensions (of the buffer layers), since they

usually depend on the dimensions of the entire semiconductor component.

Applicant further believes that the Examiner did not carry the burden of establishing a prima facie case of obviousness with respect to claim 3.

Clearly, the references do not show "another of said four doped regions being a second base region having a conductivity type with an opposite sign with respect to said given conductivity type, said second base region extending as far as said first main side, having a channel and having said gate electrode for controlling said channel; *a further buffer layer being doped to have said given conductivity type and being disposed between said first base region and said second base region, a doping of said further buffer layer having a magnitude causing the semiconductor component to block in a direction from said drain contact toward said source contact in an envisaged range of opposite applied electrical voltages*", as recited in claim 3 of the instant application (emphasis added). Thus, neither can the specific combination of the aforementioned limitations be shown. Claim 5 recites similar limitations.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either

show or suggest the features of claims 3 and 5. Claims 3 and 5 are, therefore, believed to be patentable over the art and since the dependent claim 4 is ultimately dependent on claim 3, and since the dependent claim 6 is ultimately dependent on claim 5, they are believed to be patentable as well.

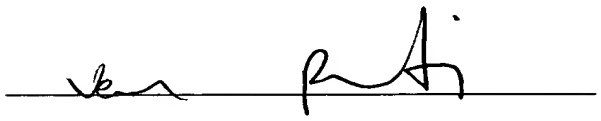
In view of the foregoing, reconsideration and allowance of claims 3-8 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, the Examiner is respectfully requested to telephone counsel so that, if possible, patentable language can be worked out.

Please charge any fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and

Greenberg, P.A., No. 12-1099.

Respectfully submitted,



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November 14, 2002

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

Claim 3 (amended). A semiconductor component, comprising:

a semiconductor body having:

first and second main sides;

four doped regions with conductivities having alternating signs formed one above another between said first and second main sides;

a gate electrode disposed on said first main side;

a source contact;

a drain contact;

one of said four doped regions being a weakly doped first base region with a given conductivity type;

another of said four doped regions being a second base region having a conductivity type with an opposite sign with respect to said given conductivity type, said second base region extending as far as said first main side [and being connected to], having a channel and having said gate electrode[, said second base region formed to control] for controlling said [a] channel [formed in said second base region];

two remaining regions of said four doped regions being respectively connected to one of said source contact and said drain contact;

said source contact being connected to said second base region and being disposed on said first main side;

a buffer layer being doped to have said given conductivity type, said buffer layer being disposed between said first base region and one of said two remaining regions connected to said drain contact;

said first base region being dimensioned and a magnitude of a doping of said buffer layer being chosen such that, in an operating state in which the semiconductor component effects blocking in a direction from said source contact toward said drain contact, at least in an envisaged range of applied electrical voltages, a space charge zone present in said first

base region is formed in a manner extending at least as far as said buffer layer; and

a further buffer layer being doped to have said given conductivity type and being disposed between said first base region and said second base region, [a magnitude of] a doping of said further buffer layer <u>having a magnitude</u> [being chosen such that] <u>causing</u> the semiconductor component <u>to</u> [effects blocking] <u>block</u> in a direction from said drain contact toward said source contact in an envisaged range of opposite applied electrical voltages.

Claim 5 (amended). A semiconductor component, comprising:

a semiconductor body having:

first and second main sides;

a gate electrode disposed <u>on</u> said first main side;

a source contact;

a drain contact disposed <u>on</u> said second main side;

a first base region having a weak doping with a given conductivity type;

a second base region having a conductivity type opposite said given conductivity type and a channel, said second base region extending from said first main side into said semiconductor body[, being connected to] and having said gate electrode[, and being formed to control] for controlling said channel];

a third region having a conductivity type opposite said given conductivity type and being connected to said drain contact;

a fourth region having said given conductivity type and being connected to said second base region;

said source contact being disposed on said first main side and being connected to said fourth region and to said second base region;

a buffer layer being doped to have said given conductivity type, said buffer layer being disposed between said first base region and said third region;

a further buffer layer being doped to have said given conductivity type and being disposed between said first base region and said second base region;

said first base region being dimensioned and a magnitude of a doping of said buffer layer being chosen such that, in an operating state in which the semiconductor component effects blocking in a direction from said source contact toward said drain contact, at least in an envisaged range of applied electrical voltages, a space charge zone present in said first base region is formed in a manner extending at least as far as said buffer layer; and

[a magnitude of] a doping of said further buffer layer <u>having a magnitude</u> [being chosen such that] <u>causing</u> the semiconductor component <u>to</u> [effects blocking] <u>block</u> in a direction from said drain contact toward said source contact in an envisaged range of opposite applied electrical voltages.